

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-6, 8-9 and 11-15 are pending. Claims 1-6, 8-9 and 11-15 stand rejected.

In this response, claims 1, 13, and 15 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants respectfully submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 112

Applicants have amended claim 1 to include a substrate that has a first conductivity region and recesses, wherein the recesses have an inwardly concaved geometry with inflection points; and a silicon or silicon alloy layer in the recesses that form a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1 \times 10^{18}/\text{cm}^3$ to $3 \times 10^{21}/\text{cm}^3$ on opposite sides of said gate electrode, wherein the source/drain regions have the inwardly concaved geometry with the inflection points that is determined by the recesses.

Therefore, applicants respectfully submit that claim 1, as amended, is patentable under 35 U.S.C. § 112, first paragraph.

Because amended independent claims 13 and 15, and respective dependent claims 2-6, 8-9, 11-12, and 14 contain similar limitations, applicants respectfully submit that claims amended independent claims 13 and 15, and respective dependent claims 2-6, 8-9, 11-12, and 14 are patentable under 35 U.S.C. § 112, first paragraph.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1, 8, 9 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,060,033 to Takeuchi ("Takeuchi '033").

The Examiner stated that the limitation "recesses, wherein the recesses have an inwardly concaved geometry with inflection points;...a silicon or silicon alloy layer deposited into the recesses", ...is a product-by-process limitation..." (Office Action, p. 4, 12/14/06)

Applicants have amended claim 1 to include a substrate that has a first conductivity region and recesses, wherein the recesses have an inwardly concaved geometry with inflection points; and a silicon or silicon alloy layer in the recesses that form a pair of inwardly concaved source/drain regions of a second conductivity type having a concentration of impurities in a range of $1 \times 10^{18}/\text{cm}^3$ to $3 \times 10^{21}/\text{cm}^3$ on opposite sides of said gate electrode, wherein the source/drain regions have the inwardly concaved geometry with the inflection points that is determined by the recesses creating metallurgical inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points, which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric, and directly define a first channel region having a first metallurgical channel length directly beneath said lower portion of said gate electrode in said first conductivity type region, and a second channel region having a second metallurgical length between said metallurgical inflection points, wherein said first metallurgical channel length directly beneath said lower portion of said gate electrode is larger than said second metallurgical channel length between said metallurgical inflection points.

Applicants respectfully submit that limitations “a substrate that has a first conductivity region and recesses, wherein the recesses have an inwardly concaved geometry with inflection points”, as recited in amended claim 1 are disclosed in the subject Specification (for example, Figure 6, p. 16, lines 1-19). Applicants respectfully submit that limitations “ a silicon or silicon alloy layer in the recesses that form a pair of inwardly concaved source/drain regions, wherein the source/drain regions have the inwardly concaved geometry with the inflection points that is determined by the recesses,” as recited in amended claim 1 are disclosed in the subject Specification (for example, in Figure 2, p. 9, line 6-p. 10, line 13; and Figure 7).

The Examiner acknowledged that “Takeuchi’033 does not disclose an inflection point which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-100Å beneath said gate dielectric” (Office Action, p. 3, 12/14/06).

Takeuchi’033 discloses a MOS transistor (Figure 1h). In particular, Takeuchi’033 discloses

FIG. 1(h) is a cross-sectional view of an MOS transistor in a final process in accordance with the present invention. As shown in FIG. 1(h), the MOS transistor in accordance with the present invention comprises a semiconductor substrate 101, e.g., a p-type silicon substrate; an element isolating separating insulation film 102, e.g., a silicon oxide film; an insulating film 103, such as a gate insulating film constituted by a silicon oxide film; a p-type layer 104 having an impurity concentration higher than that of silicon substrate 101; a gate electrode 105; source and drain regions 106 formed by an n-type layer of low-concentration impurities; a side wall insulating film 108 formed from a silicon oxide film 107 or the like; and source and drain regions 109 formed by an n-type layer of high-concentration impurities. (col. 3, lines 50-67) (emphasis added)

Further, Takeuchi’033 discloses

Thus, Takeuchi’033 merely discloses a transistor having a substrate. Takeuchi’033 fails to disclose, teach, or suggest a substrate that has recesses, wherein the recesses have an inwardly concaved geometry with inflection points, as recited in amended claim 1.

Furthermore, Takeuchi'033 merely discloses that the source and drain regions are formed by the n-type layer. In contrast to the source/drain regions have the inwardly concaved geometry with the inflection points that is determined by the recesses in the substrate, as recited in amended claim 1.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033.

Because claims 8, 9, and 11 depend from amended claim 1, and add additional limitations, Applicants respectfully submit that claims 8, 9, and 11 are not obvious under 35 U.S.C. § 103(a) over Takeuchi'033.

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, and further in view of U.S. Patent No. 5,970,351 to Takeuchi ("Takeuchi '351").

Takeuchi'351 discloses elevated drain/source regions formed on a substrate, and similarly to Takeuchi'033, fails to disclose the discussed limitations of amended claim 1.

Thus, neither Takeuchi'033, Takeuchi'351, nor any combination thereof discloses source/drain regions that have the inwardly concaved geometry with the inflection points that is determined by the recesses in the substrate, as recited in amended claim 1.

Therefore, Applicants respectfully submit that claim 2 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Takeuchi'351.

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi'033, in view of U.S. Patent No. 6,057,582 to Choi ("Choi '582").

Choi'582 discloses a transistor having a gate insulating film having thicknesses at both sides thicker than a thickness at a center formed on semiconductor substrate 21, and similarly to Takeuchi'033 and Takeuchi'351, fails to disclose the discussed limitations of amended claim 1.

Because claim 3 contains the discussed limitations, Applicants respectfully submit that claim 3 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033 in view of Choi'582.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, in view of Takeuchi '351, and further in view of Choi '582.

As set forth above, neither Takeuchi'033, Takeuchi'351, Choi'582, nor any combination thereof, discloses the discussed limitations of amended claim 1.

Because claim 4 depends from amended claim 1 and add additional limitations, Applicants respectfully submit that claim 4 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Takeuchi'351, and further in view of Choi'582.

Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, and further in view of U.S. Patent No. 5,793,088 to Choi et al. ("Choi '088").

Choi'088 discloses controlling the threshold voltage by providing a threshold voltage implant into the edges of the halo regions, and similarly to Takeuchi'033, does not disclose the discussed limitations of amended claim 1.

Because claims 5 and 6 depend from amended claim 1 and add additional limitations, Applicants respectfully submit that claims 5 and 6 are not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Choi'088.

Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033, and further in view of U.S. Patent No. 5,567,966 to Hwang ("Hwang").

Hwang discloses thinning the channel region by local oxidation and wet etch, and similarly to Takeuchi'033, fails to disclose the discussed limitations of amended claim 1. Thus, neither Takeuchi'033, Hwang, nor a combination thereof, discloses such limitations of amended claim 1.

Because claim 12 depends from amended claim 1, Applicants respectfully submit that claim 12 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Hwang.

Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of U.S. Patent No. 6,274,894 to Wieczorek et al. ("Wieczorek") in view of Takeuchi '351.

Wieczorek discloses forming low-bandgap source and drain regions for MOS transistors, and similarly to Takeuchi'033 and Takeuchi'351, fails to disclose the discussed limitations.

Because claim 13 contains the discussed limitations, Applicants respectfully submit that claim 13 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek, and further in view of Takeuchi'351.

Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi '582.

As set forth above, neither Takeuchi'033, Wieczorek, Takeuchi'351, Choi'582, nor a combination thereof, discloses the discussed limitations.

Because claim 14 depends from amended claim 13, Applicants respectfully submit that claim 14 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek, in view of Takeuchi'351, and further in view of Choi'582.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '033 in view of Wieczorek.

As set forth above, neither Takeuchi'033, Wieczorek, nor a combination thereof, discloses the discussed limitations.

Because amended claim 15 contains the discussed limitations, Applicants respectfully submit that amended claim 15 is not obvious under 35 U.S.C. § 103(a) over Takeuchi'033, in view of Wieczorek.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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By: _____



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